Curriculum Vitae

Danella Zhao

Dept. of Electrical & Computer Engineering
University of Arizona
Danella@Google Scholar

Phone: (520)621-6192
Email: danellazhao@arizona.edu
Website: http://www.u.arizona.edu/∼danellazhao

1 Education

- Feb. 2004 : Ph.D., Department of Computer Science and Engineering, State University of New York at Buffalo. Dissertation: *"An Integrated Framework for Concurrent Test and Wireless Control in Complex SoCs"*. Advisor: Professor Shambhu Upadhyaya.
- June 2001 : M.S., Department of Computer Science and Engineering, State University of New York at Buffalo. Project: *"Impact of Copper Interconnect on Pipelining and Synchronization"*. Advisor: Professor Ramalingam Sridhar.
- June 1996 : B.S., Department of Biomedical Engineering and Instrumentation, Zhejiang University, China.

2 Academic and Industrial Experience

- July 2022-presentt : *Expert*, CISE/CCF, National Science Foundation.
- June 2022-presentt : *Associate Professor*, Department of Electrical and Computer Engineering, University of Arizona.
- July 2016-May 2022 : *Graduate Program Director & Associate Professor*, Department of Computer Science, Old Dominion University.
- Aug. 2010-Jul. 2016 : *Lockheed Martin Endowed Associate Professor*, Center for Advanced Computer Studies, Univ. of Louisiana at Lafayette.
- Aug. 2004-Aug. 2010 : *Assistant Professor*, Center for Advanced Computer Studies, UL at Lafayette.
- May 2006-Jul. 2006 : *Visiting Assistant Professor and JSPS Research Fellow*, Graduate School of Information Science, Nara Institute of Science and Technology, Japan.
- Jan. 2002-Aug. 2003 : *Research Assistant*, IBM Sponsored Electronic Test Design Automation Lab, Department of Computer Science and Engineering, State University of New York at Buffalo.
- Jun. 2002-Aug. 2002 : *Research Associate*, Center for Advanced Computer Studies, UL Lafayette.
- Aug. 2003-Dec. 2003 and Aug. 1999-Dec. 2001 : *Teaching Assistant*, Department of Computer Science and Engineering, University at Buffalo.
- Jun. 2000-Aug. 2000 : *Summer Internship*, CompSys Technologies Inc., Buffalo, NY.
- Jun. 1999-Aug. 1999 : *Research Assistant*, High Performance VLSI Systems and Architecture Lab, Department of Computer Science and Engineering, University at Buffalo.
- Jul. 1996-Dec. 1998 : *System Engineer*, Zhejiang Yaojiang Group, China.

3 Research

My research focuses around the broad theme of high performance secure and intelligent nanocomputing, spanning such topics as multicore/many-core computing and on-chip networking, Internet-of-Things (IoT) intelligence & security, hardware security, autonomic computing, and machine learning. I am one of the pioneers on the research of *wireless Network-on-Chip*, a new communication paradigm for building energy-efficient many-core chips. Based on this research, I received the prestigious NSF CAREER award. My current interests center on specialized computing for machine learning and AI, encrypted computing and privacy-preserving edge computing, and machine learning-enabled computer architecture design.

3.1 Awards and Honors

- Best Student Paper Award in The 30th IEEE Microelectronics Design and Test Symposium (MDTS) 2021.
- University of Louisiana at Lafayette Research Excellence Award, 2013.
- Lockheed Martin Corporation/BORSF Endowed Professorship in Computer Science/Computer Engineering, 2012-2016.
- Louisiana Board of Regents Commendation for Teacher-Scholar, 2009.
- National Science Foundation Faculty Early Career Development Award, 2009.
- Best Paper Nomination in The 12th IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC) 2007.
- Japan Society for Promotion of Science (JSPS) Research Fellowship Award, 2006.
- Best Paper Award in The 12th IEEE North Atlantic Test Workshop (NATW) 2003.

3.2 Research Grants and Proposals

My research has been supported by NSF, NSA, ONR, DoD, Commonwealth Cybersecurity Initiative (CCI), EPSCoR, Louisiana Board of Regents Research Competitiveness Subprogram (RCS) and Enhancement program that total more than $5.76 million. I currently serve as PI/Co-PI on ten active federal and state grants.

Funded Projects:

(1) "Intelligent Learning in Cyber Defense", *NSA*, $175,000, 2022-2024, **PI**.

(2) "Combination Experiential Learning in Cyber Defense", *NSA/ONR*, $175,000, 2021-2023, **PI/PD**.

(3) "Cybersecurity+AI: a GenCyber Camp in the Age of AI to Train K-12 Teachers for Classroom Teaching of Cybersecurity", *NSA/ONR*, $145,398, 2021-2023, **Co-PI**.

(4) "Tangram: Scaling into the Exascale Era with Reconfigurable Aggregated Virtual Chips", *NSF*, $493,999, 2020-2023, **PI/PD** (collaborative with UNT and WSU).

(5) "A Minimum Viable Product to Secure IoT Devices through Power Auditing and Privacy Preserved Convolutional Neural Networks", *CCI Innovative Bridge Fund*, $50,000, 2021-2022, **Co-PI** (Williams & Mary lead).

(6) "DoD CyberSP Program", *NSA*, $315,908, 2021-2022, **Co-PI**.

(7) "DeepPOSE: Securing Transportation Systems from GPS Spoofing Attack", *CCI*, $200,000, 2021-2022, **Co-PI** (collaborative with VCU and Virginia Tech).

(8) "Sensor Degradation Detection Algorithm for Automated Driving Systems", *CCI*, $200,000, 2021-2022, **Co-PI** (Virginia Tech lead).

(9) "Students and Teachers Interactive Learning in Cyber Defense", *NSA/ONR*, $125,000, 2021-2022, **PI/PD**.

(10) "Building Cybersecurity Inclusive Pathways towards Higher Education and Research (CIPHER)", *NSF*, $100,000, 2020-2022, **Co-PI**.

(11) "Preparing JROTC Students to Defend the Cyberspace", *NSA/NSF*, $100,000, 2020-2022, **PI/PD**.

(12) "Securing IoT Devices through Power Side Channel Auditing and Privacy Preserved Convolutional Neural Networks", *CCI*, $150,000, 2020-2021, **Co-PI** (Williams & Mary lead).

(13) "Developing Cyber Talents to Secure DoD Cyberspace", *DOD*, $71,782, 2020-2021, **Co-PI**.

(14) "Preparing Tomorrow's Heros to Secure the Cyberspace", *NSA/NSF*, $100,000, 2019-2020, **Co-PI**.

(15) "MRI Acquisition: A Reconfigurable Computing Infrastructure Enabling Interdisciplinary and Collaborative Research in Hampton Roads", *NSF MRI*, $1,504,396 (plus $451K institute match), 2018-2021, **Senior Personnel**.

(16) "Wireless Network-on-Chip: A New Communication Paradigm for Heterogeneous Gigascale MPSoCs", *NSF Career*, $621,230, 2009-2015, **PI/PD**.

(17) "A Wireless Nanonetworks Integration and Emulation System for Multi-Processor SoC Research and Education", *NSF MRI*, $500,000 (plus $214K institute match), 2008-2013, **PI/PD**.

(18) "Intra-chip Wireless Nanonetworks for High-Performance Embedded Computing", *EPSCoR/Pfund*, $10,000, 2008-2009, **PI/PD**.

(19) "The Design of Communication-Centric Embedded System-on-Chips", *Louisiana BoRSF Enhancement*, $99,642 (plus $5,000 institute match), 2007-2009, **PI/PD**.

(20) "On-chip RF/Wireless Interconnect Technology in Nanometer Design", *Louisiana BoRSF RCS*, $99,705, 2005-2009, **PI/PD**.

(21) "Industry-Academia Innovation Forum - The Future of AI and Autonomous Driving", *IEEE CASS Outreach Initiative 2017 grant*, $8,000, 2017, **Organizer**.

(22) "IEEE Outreach Workshop on Multicore/Many-core SoC Design & Development", *IEEE CASS Outreach Initiative 2015 grant*, $5,000, 2015, **Organizer**.

(23) "SoC Tech Tutorial School", IEEE CAS Society Outreach Initiative 2014 grant, $16,000, 2014, **Organizer**.

Pending Proposal:

(24) "NSF INCLUDES Alliance: Cybersecurity Inclusive Pathways towards Higher Education and Research (CIPHER)", *NSF*, $7,929,405, 2022-2027, **Co-PI**.

(25) "Training Cyber Talents for DoD Workforce", *DoD*, $686,680, 2022-2023, **Co-PI**.

3.3 Selected Publications and Products

Patent:

(1) Co-inventor, "A Privacy-Preserving Online Botnet Classification System Utilizing Power Footprint of IoT Connected Devices", filed for patent application, 2021.

Refereed Journal/Conference/Workshop Paper:

(2) Z. Li and D. Zhao, "ThingNet: A Lightweight Real-time Mirai IoT Variants Hunter through CPU Power Fingerprinting", in 25th Design, Automation and Test in Europe Conference (DATE), Mar. 14-23, 2022.

(3) W. Jung, Y. Feng, S. A. Khan, C. Xin, D. Zhao and G. Zhou, "DeepAuditor: Distributed Online Intrusion Detection System for IoT devices via Power Side-channel Auditing", in 21st ACM/IEEE Conference on Information Processing in Sensor Networks (IPSN), May 4-6, 2022.

(4) M.F. Reza, D. Zhao and M. Bayoumi, "Energy-Efficient Task-Resource Co-Allocation and Heterogeneous Multi-Core NoC Design in Dark Silicon Era", in Elsevier journal of Microprocessors and Microsystems, Vol. 86, Oct. 2021.

(5) Z. Li, B. Perez, S. A. Khan, B. Feldhaus and D. Zhao, "A New Design of Smart Plug for Real-time IoT Malware Detection", in Proceedings of 30th IEEE Microelectronics Design & Test Symposium (MDTS), pp. 1-6, 2021. (**Best Student Paper Award**).

(6) R. Galledari and D. Zhao, "Deep Reinforcement Learning for UAV Battery Lifetime Prediction - On the Perspective of On-the-Fly Wireless Charging", in ACM Capital Region Celebration of Women in Computing (CAPWIC) 2019, Mar. 22-23, 2019.

(7) Md F. Reza, D. Zhao, H. Wu, and M. Bayoumi, "Hotspot-Aware Task-Resource Co-allocation for Heterogeneous Many-core Networks-on-Chip", in Elsevier Journal of Computers & Electrical Engineering, Vol. 68, May 2018, pp. 581-602.

(8) Md F. Reza, D. Zhao, and M. Bayoumi, "Power-Thermal Aware Balanced Task-Resource Co-Allocation in Heterogeneous Many CPU-GPU Cores NoC in Dark Silicon Era", in Proceedings of *31st IEEE International System-on-Chip Conference (SOCC)*, Washington DC, Sept. 5-8, 2018.

(9) Md F. Reza, T.T. Le, B. Dey, M. Bayoumi, and D. Zhao, "Neuro-NoC: Energy Optimization in Heterogeneous Many-Core NoC Using Neural Networks in Dark Silicon Era", in Proceedings of *51st IEEE International Symposium on Circuits and Systems (ISCAS)*, Florence, Italy, May 27-30, 2018.

(10) T.T. Le, R. Ning, D. Zhao, H. Wu, and M. Bayoumi, "Optimizing the Heterogeneous Network On-Chip Design in Manycore Architectures", in Proceedings of *30th IEEE International System-on-Chip Conference (SOCC)*, pp. 184-189, Sept. 5-8 2017, Munich, Germany.

(11) M. Bai, D. Zhao, and M. A. Bayoumi, "Router-level Performance Driven Dynamic Management in Hierarchical Networks-on-Chip", in Proceedings of *30th IEEE International System-on-Chip Conference (SOCC)*, pp. 310-315, Sept. 5-8 2017, Munich, Germany.

(12) T.T. Le, D. Zhao, and M. Bayoumi, "Efficient Reconfigurable Global Network-on-chip Designs towards Heterogeneous CPU-GPU Systems: An Application-Aware Approach", in Proceedings of *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, pp. 439-444, July 2017, Bochum, Germany.

(13) Md F. Reza, D. Zhao, and M. Bayoumi, "Dark Silicon-Power-Thermal Aware Runtime Mapping and Configuration in Heterogeneous Many-Core Chip", in Proceedings of *50th IEEE International Symposium on Circuits and Systems (ISCAS)*, Baltimore, Maryland, May 28-31, 2017.

(14) M. Bai, D. Zhao, and M. Bayoumi, "Dynamic Congestion Reduction Among Hierarchical Networks-on-Chip", in Proceedings of *50th IEEE International Symposium on Circuits and Systems (ISCAS)*, Baltimore, Maryland, May 28-31, 2017.

(15) A. Rezaei, M. Daneshtalab, and D. Zhao, "CAP-W: Congestion-Aware Platform for Wireless-based Network-on-Chip in Many-Core Era", In *Elsevier Journal of Microprocessors and Microsystems (MICPRO-Elsevier)*, Vol. 52, pp. 23-33, 2017.

(16) A. Rezaei, D. Zhao, M. Daneshtalab, and H. Zhou, "Multi-Objective Task Mapping Approach for Wireless NoC in Dark Silicon Age", in Proceedings of *25th IEEE Euromicro International Conference on Parallel, Distributed and Network-Based Computing (PDP)*, St. Petersburge, Russia, Mar. 6-8, 2017.

(17) M. Bai, D. Zhao, and H. Wu, "CATBR-Congestion Aware Traffic Bridging Routing Among Hierarchical Networks-on-Chip", in Proceedings of *29th IEEE International System-on-Chip Conference (SOCC)*, Seattle, WA, Sept. 6-9, 2016.

(18) A. Rezaei, M. Daneshtalab, D. Zhao, and M. Modarressi, "SAMi: Self-Aware Migration Approach for Congestion Reduction in NoC-based MCSoC", in Proceedings of *29th IEEE International System-on-Chip Conference (SOCC)*, Seattle, WA, Sept. 6-9, 2016.

(19) S. Maabi, F. Safaei, A. Rezaei, M. Daneshtalab, and D. Zhao, "ERFAN: Efficient Reconfigurable Fault-Tolerant Deflection Routing Algorithm for 3-D Network-on-Chip", in Proceedings of *29th IEEE International System-on-Chip Conference (SOCC)*, Seattle, WA, Sept. 6-9, 2016.

(20) A. Rezaei, D. Zhao, M. Daneshtalab, and H. Wu, "Shift Sprinting: Fine-Grained Temperature-Aware NoC-based MCSoC Architecture in Dark Silicon Age", in *53rd IEEE/ACM Design Automation Conference (DAC)*, Austin, TX, June 6-9, 2016.

(21) F. Reza, D. Zhao and H. Wu, "Task-Resource Co-Allocation for Hotspot Minimization in Heterogeneous Many-Core NoCs", in 26th ACM Great Lakes Symposium VLSI (GLSVLSI), Boston, MA, May 2016.

(22) A. Rezaei, M. Daneshtalab, F. Safaei and D. Zhao, "Hierarchical Approach for Hybrid Wireless Network-on-Chip in Many-core Era", in *Elsevier Journal of Computers and Electrical Engineering*, Vol. 51, Num. C, pp. 225-234, Apr. 2016.

(23) A. Rezaei, M. Daneshtalab, M. Palesi and D. Zhao, "Efficient Congestion-Aware Scheme for Wireless On-Chip Networks", in proceedings of *24th Euromicro International Conference on Parallel, Distributed and Network-Based Processing (PDP)*, pp. 742-749, Heraklion Crete, Greece, Feb. 17-19, 2016.

(24) A. Rezaei, M. Daneshtalab, D. Zhao, F. Safaei, X. Wang and M. Ebrahimi, "Dynamic Application Mapping Algorithm for Wireless Network-on-Chip", in *23rd Euromicro International Conference on Parallel, Distributed and Network-Based Processing (PDP)*, pp. 421-424, Turku, Finland, Mar. 4-6, 2015.

(25) D. Zhao, Y. Wang, H. Wu and T. Kikkawa, "$I(Re)^2$-WiNoC: Exploring Scalable Wireless On-Chip Micronetworks for Heterogeneous Embedded Many-Core SoCs", in *Elsevier Journal of Digital Communications and Networks*, Vol. 1, No. 1, pp. 45-56, Feb. 2015.

(26) U. Chandran and D. Zhao, "Cost-Optimal Design of Wireless Pre-bonding Test Framework", in *27th IEEE International System-on-Chip (SOCC)*, Las Vegas, NV, Sept. 2-5, 2014.

(27) R. Wu and D. Zhao, "Load Adaptive Multi-Channel Distribution and Arbitration in Unequal RF Interconnected WiNoC", in *45th IEEE International Symposium on Circuits and Systems (ISCAS)*, Melbourne, Australia, June 1-5, 2014.

(28) R. Wu and D. Zhao, "Integrated Routing and Channel Arbitration in Overlaid Mesh WiNoC", in *26th IEEE International System-on-Chip Conference (SOCC)*, pp. 368-373, Erlangen, Germany, Sept. 4-6, 2013.

(29) U. Chandran, D. Zhao and R. Jayabharathi, "Hybrid 3D Pre-bonding Test Framework Design", in *IEEE European Test Symposium (ETS)*, Avignon, France, May 27-30 2013.

(30) D. Zhao and R. Wu, "Overlaid Mesh Topology Design and Deadlock Free Routing in Wireless Network-on-Chip", in *IEEE International Symposium on Networks-on-Chips (NOCS)*, pp. 27-34, Lyngby Denmark, May 9-11 2012.

(31) Y. Wang, D. Zhao and J. Li, "DuSCA: A Multi-Channeling Strategy for Doubling Communication Capacity in Wireless NoC", in *IEEE International Conference on Computer Design (ICCD)*, pp. 75-80, Montreal, Canada, Sept. 30-Oct. 3 2012.

(32) D. Zhao and Y. Wang, "Design of A Scalable RF Microarchitecture for Heterogeneous MPSoCs", in *IEEE International SoC Conference (SOCC)*, pp. 346-351, Niagara Falls, NY, Sept. 12-14 2012.

(33) D. Zhao, Y. Wang, J. Li and T. Kikkawa, "Design of Multi-Channel Wireless NoC to Improve On-Chip Communication Capacity", in *IEEE International Symposium on Networks-on-Chips (NOCS)*, pp. 177-184, Pittsburgh, PA, May 1-4 2011.

(34) R. Wu and D. Zhao, "Unequal RF Interconnected Wireless Network-on-Chip to Improving On-Chip Communication Performance", in *ACM/IEEE Design Automation Conference (DAC) poster session*, June 2011.

(35) R. Wu, Y. Wang and D. Zhao, "A Low-Cost Deadlock-free Design of Minimal-Table Rerouted XY-Routing for Irregular Wireless NoCs", in *IEEE International Symposium on Networks-on-Chips (NOCS)*, pp. 199-206, Grenoble, May 3-6 2010.

(36) U. Chandran and D. Zhao, "Thermal Driven Test Access Routing in Hyper-interconnected Three-Dimensional System-on-Chip", in *24th IEEE Int'l Symposium on Defect and Fault Tolerance in VLSI Systems (DFT)*, pp. 410-418, Chicago, IL, Oct. 7-9 2009.

(37) Y. Wang and D. Zhao, "Distributed Flow Control and Buffer Management for Wireless Network-on-Chip", in *The IEEE International Symposium on Circuits and Systems (ISCAS)*, Taiwan, May 2009.

(38) U. Chandran and D. Zhao, "SS-KTC: A High-Testability Low-Overhead Scan Architecture with Multi-Level Security Integration", in *27th IEEE VLSI Test Symposium (VTS)*, pp. 321-326, Santa Cruz, CA, May 3-7 2009.

(39) U. Chandran and D. Zhao, "Thermal Safe Modular Testing of Three-Dimensional System-on-Chip", in *IEEE North Atlantic Test Workshop (NATW)*, May 2009.

(40) D. Zhao and Y. Wang, "SD-MAC: Design and Synthesis of A Hardware-Efficient Collision-Free QoS-Aware MAC Protocol for Wireless Network-on-Chip", in *IEEE Transactions on Computers (TC)*, Vol. 57, No. 9, PP. 1230-1245, Sept. 2008.

(41) D. Zhao and Y. Wang, "MTNet: Design and Integration of A Wireless Test Framework for Heterogeneous Nanometer Systems-on-Chip", in *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, Vol. 16, No. 8, pp. 1046-1057, Aug. 2008.

(42) T. E. Yu, T. Yoneda, D. Zhao and H. Fujiwara,, "Effective Domain Partitioning for IP Core Wrapper Design Under Power Constraints", in *IEICE Transactions on Information and Systems*, Vol. E91-D, No.3, pp. 807-814, 2008.

(43) D. Zhao, "Ultraperformance Wireless Interconnect Nanonetworks for Heterogeneous Gigascale Multi-Processor SoCs", in *2nd Workshop on Chip Multiprocessor Memory Systems and Interconnects (CMP-MSI)*, in conjunction with the 35th Int'l Symp. on Computer Architecture, June 2008.

(44) Y. Wang and D. Zhao, "The Design and Synthesis of A Synchronous and Distributed MAC Protocol for Wireless Network-on-Chip", in *The 25th IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pp. 612-617, San Jose, CA, Nov. 2007.

(45) D. Zhao, R. Huang and H. Fujiwara, "Multi-Frequency Modular Testing of SoCs by Dynamically Reconfiguring Multi-port ATE", in *The 16th IEEE Asian test Symposium (ATS)*, pp. 107-110, Beijing, China, Oct. 2007.

(46) D. Zhao, Y. Wang and H. Wu, "Dual-Channel Binary-Countdown Medium Access Control in Wireless Network-on-Chip", in *IEEE/ACM International Conference on Nano-Networks (Nano-Net)*, Catania, Italy, Sept. 2007.

(47) Y. Wang and D. Zhao, "Design and Implementation of Routing Scheme for Wireless Network-on-Chip", in *The 38th IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1357-1360, New Orleans, LA, May 2007.

(48) D. Zhao, R. Huang, T. Yoneda and H. Fujiwara, "Power-Aware Multi-Frequency Heterogeneous SoC Test Framework Design with Floor-Ceiling Packing", in *The 38th IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 2942-2945, New Orleans, LA, May 2007.

(49) T. E. Yu, T. Yoneda, D. Zhao and H. Fujiwara, "Using Domain Partitioning in Wrapper Design for IP Cores Under Power Constraints", in *The 25th IEEE VLSI Test Symposium (VTS)*, pp. 369-374, May 2007.

(50) D. Zhao, U. Chandran and H. Fujiwara, "Shelf Packing to the Design and Optimization of A Power-Aware Multi-Frequency Wrapper Architecture for Modular IP Cores", in *The 12th IEEE Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp. 714-719, Yokohama, Japan, Jan. 2007. (**Best Paper Candidate**)

(51) D. Zhao, S. Upadhyaya and M. Margala, "Design of A Wireless Test Control Network with Radio-on-Chip Technology for Nanometer Systems-on-Chip", in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 25, No. 7, pp. 1411-1418, July 2006.

(52) T. E. Yu, T. Yoneda, D. Zhao and H. Fujiwara, "Designing Power-Aware Wrapper for Multi-Clock Domain Cores Using Clock Domain Partitioning", in *The 7th IEEE International Workshop on RTL and High Level Testing (WRTLT)* in conjunction with ATS'06, pp.43-48, Nov. 2006.

(53) D. Zhao and Y. Wang, "MTNet: Design and Optimization of A Wireless SoC Test Framework", in *The 19th IEEE International SoC Conference (SOCC)*, pp. 239-242, Austin, TX, Sept. 2006.

(54) D. Zhao and U. Chandran, "Design of A Time-Gated Multi-Frequency Wrapper Architecture for Modular SoC Testing", in *The 15th IEEE North Atlantic Test Workshop (NATW)*, pp. 71-78, Essex Junction, VT, May 2006.

(55) D. Zhao and Y. Wang, "A Hybrid SoC Test Model with Reconfigurable Wireless Routing", in *The 13th IEEE International Test Synthesis Workshop (ITSW)*, Santa Barbara, CA, April 2006.

(56) D. Zhao and S. Upadhyaya, "Dynamically Partitioning Test Scheduling with Adaptive TAM Configuration for Power-constrained SoC Testing", in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 24, No. 6, pp. 956-965, June 2005.

(57) D. Zhao, S. Upadhyaya and M. Margala, "A New SoC Test Architecture with RF/Wireless Connectivity", in *The 10th IEEE European Test Symposium (ETS)*, pp. 14-19, Tallinn, Estonia, May 2005.

(58) D. Zhao and S. Upadhyaya, "A Generic Resource Distribution and Test Scheduling Scheme for Embedded Core Based SoCs" in IEEE Transactions on Instrumentation and Measurement (TIM), Vol.53, No.2, pp. 318-329, April 2004.

(59) D. Zhao, S. Upadhyaya and M. Margala, "Control Constrained Resource Partitioning for Complex SoCs", in *The 18th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (DFT)*, PP. 425-432, Cambridge, MA, Nov. 2003.

(60) D. Zhao and S. Upadhyaya, "A Resource Balancing Approach to SoC Test Scheduling", in *The 34th IEEE International Symposium on Circuits and Systems (ISCAS)*, Vol. 5, pp. 525-528, Bangkok, Thailand, May 2003.

(61) D. Zhao, S. Upadhyaya and M. Margala, "A New Distributed Test Control Architecture with Multihop Wireless Test Connectivity and Communication for GagaHerze Systems-on-Chip", in *The 12th IEEE North Atlantic Test Workshop (NATW)*, PP. 76-83, Montauk, NY, May 2003. (**Best Paper Award**).

(62) D. Zhao and S. Upadhyaya, "Power Constrained Test Scheduling with Dynamically Varied TAM", in *The 21th IEEE VLSI Test Symposium (VTS)*, pp.273-278, Napa Valley, CA, April 2003.

(63) D. Zhao and S. Upadhyaya, "Adaptive Test Scheduling in SoCs by Dynamic Partitioning", in *The 17th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (DFT)*, PP. 334-342, Nov. 2002.

(64) D. Zhao and S. Upadhyaya, "Dynamically Partitioned Test Scheduling for SoCs Under Power Constraints", in *The 11th IEEE North Atlantic Test Workshop (NATW)*, PP. 72-81, Montauk, NY, May 2002.

(65) D. Zhao, S. Upadhyaya and M. Margala, "Minimizing Concurrent Test Time in SoCs by Balancing Resource Usage", in *The 12th ACM Great Lakes Symposium on VLSI (GLSVLSI)*, PP. 77-82, NYC, NY, April 2002.

Journal/Conference Paper Under Review:

(66) S.A. Khan, Q. Zhang, Z. Li, W. Jung, Y. Feng, and D. Zhao, C. Xin, and G. Zhou, "EAGLE: Lightweight Privacy-Preserving Inference for Real-Time IoT Botnet Detection", submitted to DSN'2022.

(67) S.A. Khan, Q. Zhang, Z. Li, D. Zhao, "EAGLE-Net: 2-Party Secure Computation for Neural Network Training to Detect IoT Botnet", submitted to IJCAI'2022.

Technical Report:

(68) D. Zhao and Y. Wang, "Application-Specific Design of Wireless Network-on-Chip with Geographic Routing for Gigascale MPSoCs", technical report TR-2007-8-001, the Center for Advanced Computer Studies, UL Lafayette, March 2007.

(69) T.E. Yu, T. Yoneda, D. Zhao, and H. Fujiwara, "Power Constrained IP Core Wrapper Design with Partitioned Clock Domains", IEICE Technical Report, Vol. 107, No. 103, pp. 37-42, June 2007.

(70) D. Zhao and U. Chandran, "Design and Optimization of A Time-Gated Multi-Frequency Wrapper Architecture for Embedded IP Cores", technical report TR-2006-8-001, the Center for Advanced Computer Studies, UL Lafayette, Feb. 2006.

3.4 Invited Talks

(1) "Reconfigurable Wireless Multi-chiplet Networking: A 'Transformer' to Exascale AI Chips", Keynote Speaker in 14th Network-on-Chip Architecture workshop (NoCArc) in conjunction with IEEE/ACM MICRO, Oct. 2021.

(2) "A Battle with Mirai Botnet over Internet of Things", invited talk in College of Sciences "Science Fridays" Series, Oct. 2021.

(3) "A Research Journey on Internet of Things", invited talk in Center for excellence in Education (CEE) "Virtual Bite of Science" Series, Mar. 2021.

(4) "Experiential Learning of Cyber Defense in Old Dominion GenCyber", invited talk in Annual NSA GenCyber Fall Meeting, Oct. 2020.

(5) "Shift Sprinting for Energy Efficient Computing in Dark Silicon", invited talk in College of Information Science & Electronic Engineering, Zhejiang University, China, July 2016.

(6) "Wireless Testing with Inductive Coupling", Elevator talk in 32nd IEEE VLSI Test Symposium, April 2014.

(7) "Embedded Nanocomputing: Small Devices, Large On-chip Communication Challenges", invited talk in JSPS (Japan Society for Promotion of Science) 4th Multidisciplinary Science Forum, Feb. 2014.

(8) "Wireless Network-on-Chip", panelist speaker in 15th ACM/IEEE System Level Interconnect Prediction Workshop co-located with 50th ACM/IEEE Design Automation Conference, June 2013.

(9) "Embedded Nanocomputing: Small Devices, Large On-Chip Communication Challenges", featured speaker in the 2012 Workshop on Frontiers of Information Science and Technology (FIST), Shanghai, China, Dec. 2012.

(10) "Exploring Scalable Wireless NoC Microarchitecture for Heterogeneous MPSoCs", invited talk in Dept. of Computer Science, University of California at Los Angeles, Nov. 2009.

(11) "Ultraperformance Nanonetworking for Future Multi-Processor Chips", invited talk in Dept. of Electrical Engineering, Louisiana State University, Oct. 2009.

(12) "A New On-Chip Communication Paradigm for Boosting Multi-Processor Chip Performance", invited talk in Dept. of Physics, UL Lafayette, Sept. 2009.

(13) "Wireless Network-on-Chip: A New Communication Paradigm for Gigascale Heterogeneous MPSoCs", invited talk in Research Institute for Nanodevice and Biosystems, Hiroshima University, Japan, Sept. 2009.

(14) "Security Conscious Testing and Testability Design", invited talk in The Graduate School of Information Science, Nara Institute of Science and Technology, Japan, Sept. 2009.

(15) "An Integrated Framework for Concurrent Test and Wireless Control in Complex SoCs", NAIST-COE Seminar, JSPS Centers of Excellence (COE) program, Nara Institute of Science and Technology, Japan, June 2006.

(16) "Design of A Time-Gated Multi-Frequency Wrapper Architecture for Modular SoC Testing", invited talk in The Graduate School of Information Science, Nara Institute of Science and Technology, Japan, July 2006.

4 Teaching

I set to myself two main goals when teaching students. First, to provide students with the knowledge necessary for their future studies and career. And second, not less important, to interest them in research in high performance energy-efficient computing in general and secure intelligent nanocomputing in particular. I always strike the balance between helping students to make optimal choices in their work and at the same time providing them with enough freedom and encouragement to conduct research on their own.

I have developed a series of courses in *Computer Architecture*, *Embedded System Design* and *Computer Security*, including the computer architecture core course of CS MS program and cyber defense core course of NSACAE designated CyberOP BS program. I have mentored 6 doctoral dissertations and 14 master's thesis/projects, and served on the committee for a number of Ph.D. and M.S. students. I currently supervise six PhD students.

4.1 Current Courses Offering

(1) TBA

4.2 Prior Teaching Experience at ODU

(1) CS466/566 Principles and Practices of Cyber Defenses, in Fall.

(2) CS665 Computer Architecture, in Spring.

(3) CS725/825 IoT Security, in Fall.

(4) CS334 Computer Architecture Fundamentals, in Spring and Fall 2016-2021.

(5) CS667 Co-op Education, every semester.

(6) CS669 Internship, every semester.

(7) CS697 Independent Study in CS, every semester.

(8) CS698 Master's Project, every semester.

(9) CS699 Thesis Research, every semester.

(10) CS791/891 Graduate Seminar, every semester.

(11) CS899 Doctoral Dissertation, every semester.

(12) CS495/595 Principles and Practices of Cyber Defenses, Spring 2019-Fall 2018.

(13) CS795/895 Internet of Things Intelligence & Security, Fall 2020-2018.

(14) CS495/595 Advanced Topics on Internet of Things, Spring 2018.

(15) CS795/895 Internet of Things Security, Fall 2017.

(16) CS795/895 Embedded and Cyber Physical Systems, Spring 2017.

4.2.1 Prior Teaching Experience at UL Lafayette

(1) CMPS/EECE 430 Computer Architecture, Spring 2013-2005, Fall 2015-2013, 2011, 2009, 2006.

(2) CSCE 536 Embedded System Design, Spring 2016-2014.

(3) CMPS/EECE 598 Embedded System Design, Fall 2010, 2008, 2005.

(4) CMPS/EECE 598 SoC Design and Hardware Validation, Fall 2007-2006.

(5) CMPS/EECE 598 System-on-Chip Design and Test in Nanometer Era, Fall 2004.

(6) CSCE 639 Advanced Topics on Computer Architecture, offered in every semester Fall 2014-Spring 2016.

(7) CSCE/CMPS/EECE 679 Advanced Topics on CAD/CAM, offered in every semester Fall 2004-Spring 2016.

(8) CSCE/CMPS/EECE 590 Special Project, offered in every semester Fall 2004-Spring 2016.

(9) CMPS/EECE 595 Graduate Seminar, Spring 2011-2010, Fall 2011-2009.

(10) CSCE/CMPS/EECE 599 Thesis Research and Thesis, offered in every semester Fall 2004-Spring 2016.

(11) CSCE/CMPS/EECE 699 Dissertation Research and Dissertation, offered in every semester Fall 2004-Spring 2016.

4.3 Students Advising & Mentorship

4.3.1 Major Advisor for Ph.D. Students

(1) Yi Wang (2005-2010). Dissertation: "Design of Wireless Network-on-Chip for Improving Communication Performance of Many-Core SoCs". Employment: Xilinx Inc.

(2) Unni Chandran (2007-2012). Dissertation: "Test Framework Integration and Security Design for 2-D or 3-D SoCs". Employment: Intel Corp.

(3) Ruizhe Wu (2008-2013). Dissertation: "Design of A Wireless On-chip Interconnection Network for Gagascale Many-Core Chips". Employment: Facebook

(4) Md Farhadur Reza (2012-2017). Dissertation: "Computation and Communication Optimization in Heterogeneous Many-Core Servers-on-Chip". Employment: Assistant Professor, Dept. of Computer Science & Software Engineering, Univ. of Central Missouri.

(5) Tung Thanh Le (2013-2018). Dissertation: "Optimizing Network-on-Chip Designs for Heterogeneous Many-Core Architectures". Employment: J.D. Power

(6) Mingmin Bai (2013-2018). Dissertation: "Performance-Driven Hierarchical Design and Management of Network-on-Chip in Many-Core System". Employment: Yahoo

(7) Sabbir Ahmed Khan (2017-current). Proposal: "Lightweight Secure Multiparty Deep Learning for Botnet Attack Detection at the IoT Edge".

(8) Zhuoran Li (2018-current). Proposal: "Cross-Architecture Malware Analysis Engine via Processor Side-Channel Fingerprinting".

(9) Evan Savaria (2020-current). Explore: "Detecting Adversarial Machine Learning in UAVs via Sensor Input Spoofing Attacks".

(10) Robert Slick (2020-current). Explore: "Smart and Secure Airborne Wireless Charging System for Lab-on-a-Drone".

(11) Noah Jennings (2021-current). New Student.

(12) Bryan Perez (2021-current). New Student.

4.3.2 Major Advisor for M.S. Students

(1) Unni Chandran (2008). Project: "Multi-Frequency Wrapper Architecture Design and Optimization for Embedded Core Testing". Stay for PhD.

(2) Yi Wang (2008). Project: "Low Cost Implementation of Routing Schemes for Wireless NoC". Stay for PhD.

(3) Ruben Loganantharaj (2009). Project: "A Prediction Based Flow Control Scheme for Wireless NoC". Employment: Hewlett Packard Enterprise.

(4) Ronghua Huang (2009). Project: "Multi-Frequency SoC Test Framework Design with A New Set of Bin-Packing Schemes". Employment: VT iDirect.

(5) Ran Zhang (2010). Project: "Embedded Design of An Aircraft Robot". Employment: Baidu USA.

(6) Changfeng Li (2010). Project: "Pin-Constrained Routing to Design Automation of Digital Microfluidic Biochips".

(7) Ruochi Zhang (2011). Project: "Emulation and Prototyping of A Scalable Wireless NoC System". Employment: Apple.

(8) Zhe Cui (2011). Project: "A Wireless Padded Test Framework Design for 3D SoCs". Employment: InnoGrit Corp.

(9) Md Farhadur Reza (2014). Project: "Task-Resource Co-optimization for Manycore Chips". Stay for PhD.

(10) Ali Khayat Baheri Irani (2015). Project: "Intelligent Power Management Under Dynamic Workload in Embedded Many-core SoCs". PhD at UNC Charlotte.

(11) Amin Rezaei (2016). Project: "Shift Sprinting for Energy Efficiency in Dark Silicon". PhD at Northwestern Univ.

(12) John Ashley (2017). Project: "Real-time Planning and Mapping with Computer Vision".

(13) Evan Pierre Savaria (2019). Thesis: "Novel Use of Neural Networks to Identify and Detect Electrical Infrastructure Performance". Employment: DoD NWSC (Dahlgren).

(14) Bryan Perez (2020). Project: "An Integrated Power Monitoring Engine for Real-Time IoT Botnet Detection". Stay for PhD.

(15) Serve as the MS Exit Examination Chair for all CS MS students since 2019.

4.3.3 Committee Member for Ph.D. Students

(1) Ramy E. Aly (2006). Dissertation: "Low Power RAM Design".

(2) Nan Wang (2008). Dissertation: "High Performance System-on-Chip Communication Architecture Designs".

(3) Jose L Tecpanecatl-Xihuitl (2008). Dissertation: "Efficient Multistandard Architectures for the Next Generation of Digital Front-Ends".

(4) Charbel Akl (2008). Dissertation: "Cost-Effective Interconnect and Circuit Design Methods for High-Speed Nanometer CMOS VLSI Design".

(5) Mohsen Shaaban (2009). Dissertation: "Low Complexity Paradigm for Heterogeneous Video Transcoding in Mobile Environments".

(6) Abhijit Sil (2010). Dissertation: "Design and Analysis of Application Specific SRAM Memory for Embedded Systems".

(7) Azeez Sanusi (2011). Dissertation: "High Performance Design Methodologies for Very Large Scale Integrated Network-on-Chips".

(8) Md Ibrahim Faisal (2011). Dissertation: "A Flexible Operand Size Architecture for GF(2^m) Arithmetic Processor".

(9) Adam Wade Lewis (2012). Dissertation: "Energy Conservation and Thermal Management in High-Performance Server Architectures".

(10) Mohamed Shaker (2013). Dissertation: "Design of Front End Circuits for Low Power Ultra Wideband Receiver".

(11) Jared Tessier (2013). Dissertation: "An Energy and Spectrum Efficient Multiphase Digital Ultra-wideband Transmitter".

(12) Robert Minvielle (2013). Dissertation: "Energy Scavenging in Three Dimensional Integrated Circuits with Through Silicon Vias".

(13) Seyed Mohammad Seyed Jalali Aghdam (2015). Dissertation: "Low Power Microhotplates Using Silica Aerogel As Heat Insulator".

(14) Saeid Yasami (2015). Dissertation: "Design of Ultra Low Power LNA for Space and Medical Applications in Subthreshold Region".

(15) Anandi Dutta (2016). Dissertation:"A Smart Framework for Designing Reconfigurable Multiprocessor System-on-Chip".

(16) Nasim Nasirian (2018). Dissertation:"Probabilistic Analysis of Power-gating in Network-on-Chip".

(17) Daming Feng (2019). Dissertation: "Scalable Parallel Delaunay Image-to-Mesh Conversion for Shared and Distributed Memory Architectures".

(18) Matthew R. Kelly (2019). Dissertation: "Aggregating Private and Public Web Achieves using the Mememtity Framework".

(19) Jing Xu (2020). Dissertation: "Automatic Linear and Curvilinear Mesh Generation Driven by Validity Fidelity and Topological Guarantees".

(20) Serve on the PhD Breadth Examination Committee for Hassan Al-Maksousy 2018.

(21) Serve on the PhD Candidacy Examination Committee for Mat Kelly 2018.

(22) Serve as the PhD Candidacy Examination Committee Chair for Sabbir Ahmed Khan 2019.

(23) Serve on the PhD Candidacy Examination Committee for Yanru Xiao 2019.

5 Professional Activities and Services

I enjoy various professional activities and services, which allow me to interact with the researchers and educators around the world. I have served as the Steering Committee Chair, General Chair, TPC Chair/Co-Chair, Special Session Chair, Financial Chair, Publicity Chair, Track Chair, Session Chair, TPC member, Review Committee member for various major semiconductor and electronic design automation conferences, and served as various major journal and conference reviewers and funding proposal panelist.

As a gradaute program director, I play a key role in developing and overseeing the CS graduate programs, advising 140+ MS and 50+ PhD students, mentoring CS Graduate Students Society, chairing Graduate Committee, taking charge of scholarship and fellowship promotion, new students orientations, MS exit comprehensive exams and annual PhD progress reviews, overseeing the dissertation/thesis process, etc.

I also serve as the Old Dominion GenCyber Program Director, and serve on the College of Sciences Research Council and Commonwealth Cybersecurity Initiative (CCI) Inclusion and Diversity Committee.

5.1 Professional Membership

(1) ACM, ACM SIGDA, ACM Council on Women in Computing

(2) IEEE, IEEE Computer society, IEEE Circuit and Systems society, IEEE Communication society, IEEE Women in Engineering

(3) IEEE CAS Society Technical Committee on VLSI Systems and Applications, IEEE CASS TC on Communications, IEEE CASS TC on Nanotechnologies and GigaScale Integration

(4) Test Technology Technical Council

(5) JSPS Fellow US Alumni Association

5.2 Journal Editing

(1) Elsevier Journal on Computer Communications *Technical Committee* Member.

(2) *Journal Reviewer*: IEEE Transactions on Cloud Computing, IEEE Transactions on Parallel and Distributed Systems, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on Computers, IEEE Transactions on Reliability Special Section on Trustworthy Computing, IEEE Transactions on VLSI Systems, IEEE Transactions on Circuits and Systems, I and II, IEEE Transactions on Instrumentation and Measurement, ACM Transactions on Embedded Computing Systems, ACM Transactions on Design Automation of Electronic Systems, ACM Journal of Emerging Technologies in Computing Systems, IEEE Journal of Solid-State Circuits, IEEE Computer, IEEE Design & Test of Computers, IEEE Journal on Emerging and Selected Topics in Circuits and Systems, IEEE Internet of Things Journal, IEEE Access, IEEE Transactions on Emerging Topics in Computing, IET Journal on Computers & Digital Techniques, Integration - the VLSI Journal, Journal of Electronic Testing: Theory and Applications, Journal of Circuits, Systems, and Computers, International Journal of Ad Hoc and Ubiquitous Computing, Elsevier Journal on Nano Communication Networks, Elsevier Journal on Microprocessors and Microsystems, Elsevier Journal on Parallel Computing, Elsevier Journal on Computer Communications, Elsevier Journal on Computers & Electrical Engineering.

5.3 Conference Organization

5.3.1 Conference Chairing

(1) *Steering Committee Chair/Co-Chair*: IEEE International SoC Conference 2022-2021, 2018-2017.

(2) *General Chair*: IEEE International SoC Conference 2021, 2020, 2016.

(3) *TPC Chair*: IEEE Microelectronics Design & Test Symposium 2022, 2021.

(4) *TPC Chair*: IEEE International SoC Conference 2019, 2015, 2014.

(5) *Vice TPC Chair*: IEEE North Atlantic Test Workshop 2020.

(6) *Organizer*: Automotive SoC Forum collocated with IEEE SOCC 2017.

(7) *Organizer*: Intel OpenCL Workshop for Embedded Applications on FPGAs 2016.

(8) *Chair*: IEEE Outreach Workshop on Multicore/Many-core SoC Design & Development collocated with IEEE SOCC 2015.

(9) *Chair*: SOC Tech Tutorial School collocated with IEEE SOCC 2014.

(10) *Special Session Chair*: IEEE International SoC Conference 2018-2017.

(11) *Financial Chair*: IEEE Great Lakes Symposium on VLSI 2017, 2015.

(12) *Publicity Chair*: IEEE North Atlantic Test Workshop 2019-2018.

(13) *Special Program Chair*: 24th IEEE North Atlantic Test Workshop 2015.

(14) *Track Chair*: IEEE International SoC Conference 2013-14.

(15) *Session Chair*: ACM/IEEE Design Automation Conference 2019-2017; IEEE International Symposium on NOCs 2011, 2013, 2015; IEEE European Test Symposium 2013; IEEE International Symposium on Circuits and Systems 2007-08, 2014-16, 2021; IEEE International SoC Conference 2008, 2012-16, 2018-21.

5.3.2 Member of Technical Program Committee/ Reviewer Committee

(1) *TPC Member*: ACM/IEEE International Symposium on NoCs (NOCS) 2012-13; ACM/IEEE Design Automation Conference (DAC) 2019-2017; IEEE International Conference on Computer Communications and Networks (ICCCN) 2014-17; International Workshop on Network on Chip Architectures (NoCArc) in conjunction with IEEE/ACM International Symposium on Microarchitecture 2019-2021; IEEE Asia and South Pacific Design Automation Conference (ASPDAC) 2008-11, 2015-16; IEEE International SoC Conference (SOCC) 2007-2022; IEEE Microelectronics Design and Test Symposium (MDTS) 2021-2022; IEEE International Conference on Omni-layer Intelligent systems (COINS) 2020; IEEE Great Lakes Symposium VLSI (GLSVLSI) 2017, 2015; IEEE European Test Symposium (ETS) 2013; IEEE International Conference on ASIC (ASICCON) 2011, 2015; IEEE Computer Society Annual Symposium on VLSI (ISVLSI) 2009-12; IEEE Asia Pacific Conference on Circuits and Systems (APCCAS) 2010; IEEE International Symposium on Communications and Information Technologies (ISCIT) 2010; IEEE Asian Test Symposium (ATS) 2007-08, 2012, 2014; International Workshop on RTL and High Level Testing (WRTLT) 2007-2022; IEEE North Atlantic Test Workshop (NATW) 2006-2020; IEEE International Symposium on Intelligent Signal Processing and Communication Systems (ISPACS) 2007; International Conference on Computer Design (ICCD) 2005.

(2) *Reviewer Committee Member*: IEEE International Symposium on Circuits and Systems 2008-2021.

(3) *Best Paper Award Selection Committee Member*: International Workshop on RTL and High Level Testing 2017-2016, 2008.

(4) *Best Paper Award Selection Committee Member*: IEEE International SoC Conference 2014-20.

(5) *Best Paper Award Selection Committee Member*: IEEE Asia and South Pacific Design Automation Conference 2015.

(6) *10-Year Retrospective Most Influential Paper Award Selection Committee Member*: IEEE Asia and South Pacific Design Automation Conference 2015.

5.3.3 Conference Reviewer

I have served as reviewer for many conferences such as IEEE/ACM NOCS, IEEE/ACM DAC, IEEE/ACM ICCCN, IEEE ITC, IEEE ASP-DAC, IEEE VLSID, IEEE ISVLSI, IEEE ATS, IEEE ISCAS, IEEE DSP, IEEE DFT, IEEE SOCC, IEEE GLSVLSI, IEEE ASICON, IEEE ISPACS, IEEE MDTS, IEEE/ACM NoCArc, IEEE NATW, IEEE WRTLT, IEEE ISCIT, IEEE APCCAS, ICSEC, etc.

5.4 Funding Proposal Panelist & Reviewer

(1) Served on NSF panels.

(2) Served as NSF ad hoc reviewers.

(3) Served as Proposal Reviewer of Research Grants Council (RGC) of Hong Kong.

5.5 Community Services

(1) Serve as Old Dominion GenCyber program director and direct annual summer camps and capacity building workshops to high school students and teachers in Hampton Roads

(2) Serve on Commonwealth Cybersecurity Initiative Inclusion and Diversity Committee

5.6 Educational Services

(1) Serve as ODU Computer Science Gradaute Program Director since 2019

(2) Serve on ODU College of Science Research Council since 2017

(3) Serve on ODU College of Science Research Infrastructure Subcommittee since 2017

(4) Serve on ODU College of Science Graduate Recruitment Subcommittee since 2018

(5) Serve on ODU College of Science Research Recognition Subcommittee 2017-18

(6) Serve on ODU College of Science Award Evaluation Committee (Cheng Fund for Innovative Research, Seed Fund, Distinguished Researcher, and Early Career Distinguished Researcher)

(7) Serve on ODU Asian Caucus Executive Committee - College of Science Representative since 2016-2018

(8) Serve on ODU CS Promotion & Tenure Committee since 2017.

(9) Serve as Chair of ODU CS Graduate Committee since 2019 and as member 2017-19.

(10) Serve on ODU CS Faculty Evaluation Metrics Committee since 2017.

(11) Serve on ODU CS Award Nominations Committee since 2017.

(12) Served as an UL Lafayette Graduate Council member 2011-14.

(13) Served on the UL Lafayette Faculty Senate 2009-11.

(14) Served as an UL Lafayette Graduate Faculty Review Committee member 2011-14.

(15) UL Lafayette College of Science Peer Review Committee member 2013-16.

(16) UL Lafayette College of Science Professorship Selection Committee member 2013-14.

(17) Served as UL Lafayette CACS Computer Engineering Student Application Review Committee member 2011-2016.

(18) Served as the coordinator of UL Lafayette CACS Colloquium 2009-2011.

(19) Served as reviewer for Annual UL Lafayette IEEE-CS Student Paper Contest 2005-2014.